Document Number: MRF8P20165WH
Rev. 0, 4/2011

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF8P20165WHR3
MRF8P20165WHSR3

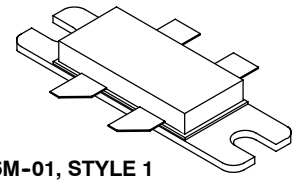
1930-1995 MHz, 37 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for base station applications with wide instantaneous bandwidth requirements covering frequencies from 1880 to 2025 MHz.

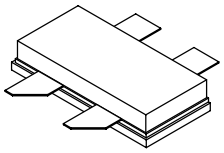
- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, P_{out} = 37 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1930 MHz	16.1	47.0	7.1	-27.7
1960 MHz	16.3	47.7	7.1	-29.7
1995 MHz	16.3	46.0	7.0	-33.3

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1960 MHz, 173 Watts CW Output Power (2 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 3 dB Compression Point ≃ 190 Watts (1)



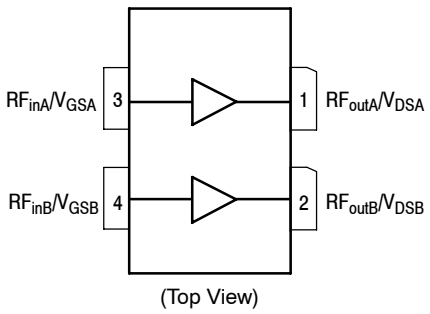
CASE 465M-01, STYLE 1
NI-780-4
MRF8P20165WHR3



CASE 465H-02, STYLE 1
NI-780S-4
MRF8P20165WHSR3

Features

- Designed for Wide Instantaneous Bandwidth Applications. VBW_{res} ≃ 100 MHz.
- Designed for Wideband Applications that Require 65 MHz Signal Bandwidth
- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Large-Signal Load-Pull Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- NI-780-4 in Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 15.
- NI-780S-4 in Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 15.



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	125	°C
Operating Junction Temperature (2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 37 W CW, 28 Vdc, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, 1960 MHz Case Temperature 114°C, 160 W CW, 28 Vdc, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, 1960 MHz	$R_{\theta JC}$	 0.79 0.53	°C/W

1. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
2. Continuous use at maximum temperature will affect MTTF.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (2)					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 232 μAdc)	$V_{GS(th)}$	1.2	1.8	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 550 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.7	3.5	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$V_{DS(on)}$	0.05	0.2	0.3	Vdc
Functional Tests (2,3,4) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, P_{out} = 37 W Avg., f1 = 1980 MHz, f2 = 2010 MHz, 2-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.8 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.2	14.8	17.2	dB
Drain Efficiency	η_D	40.6	44.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.2	5.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-31.0	-28.7	dBc

Typical Broadband Performance (4) — (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, P_{out} = 37 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1930 MHz	16.1	47.0	7.1	-27.7
1960 MHz	16.3	47.7	7.1	-29.7
1995 MHz	16.3	46.0	7.0	-33.3

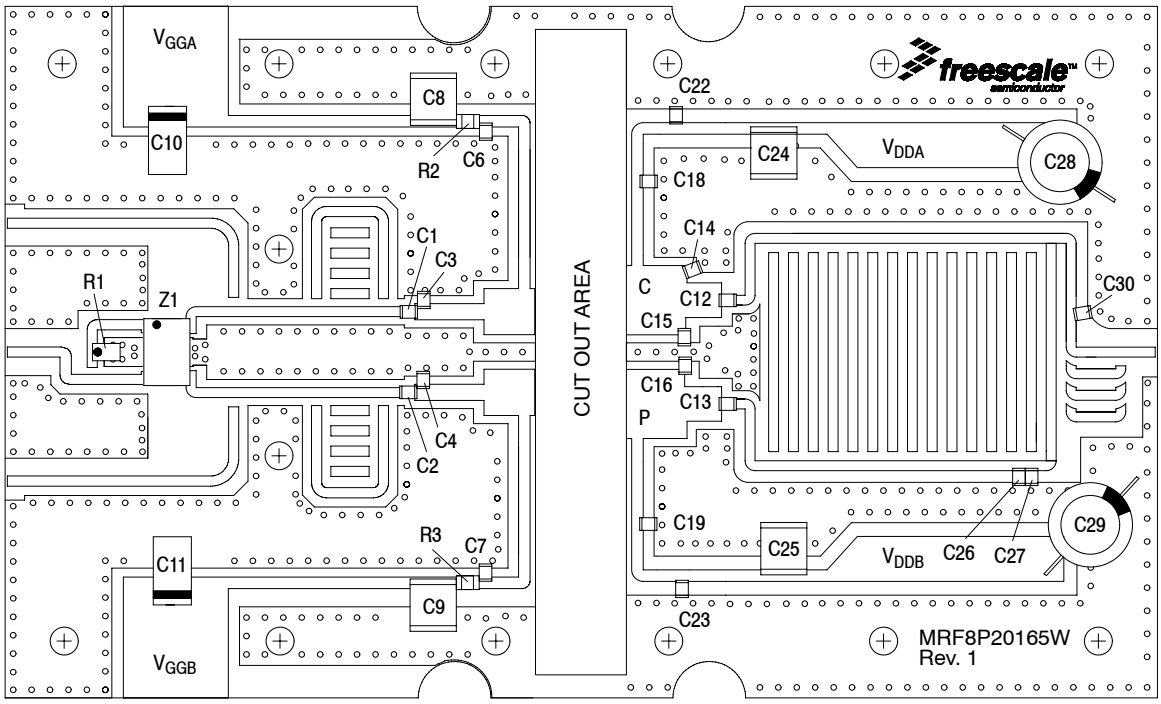
1. Side A and Side B are tied together for this measurement.
2. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
3. Part internally matched both on input and output.
4. Measurement made with device in a Symmetrical Doherty configuration.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (1) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 550 mA, V_{GSB} = 1.3 Vdc, 1930–1995 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	104	—	W
P_{out} @ 3 dB Compression Point (2)	P3dB	—	190	—	W
IMD Symmetry @ 74 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	20	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 65 MHz Bandwidth @ P_{out} = 37 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.017	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.01	—	dB/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

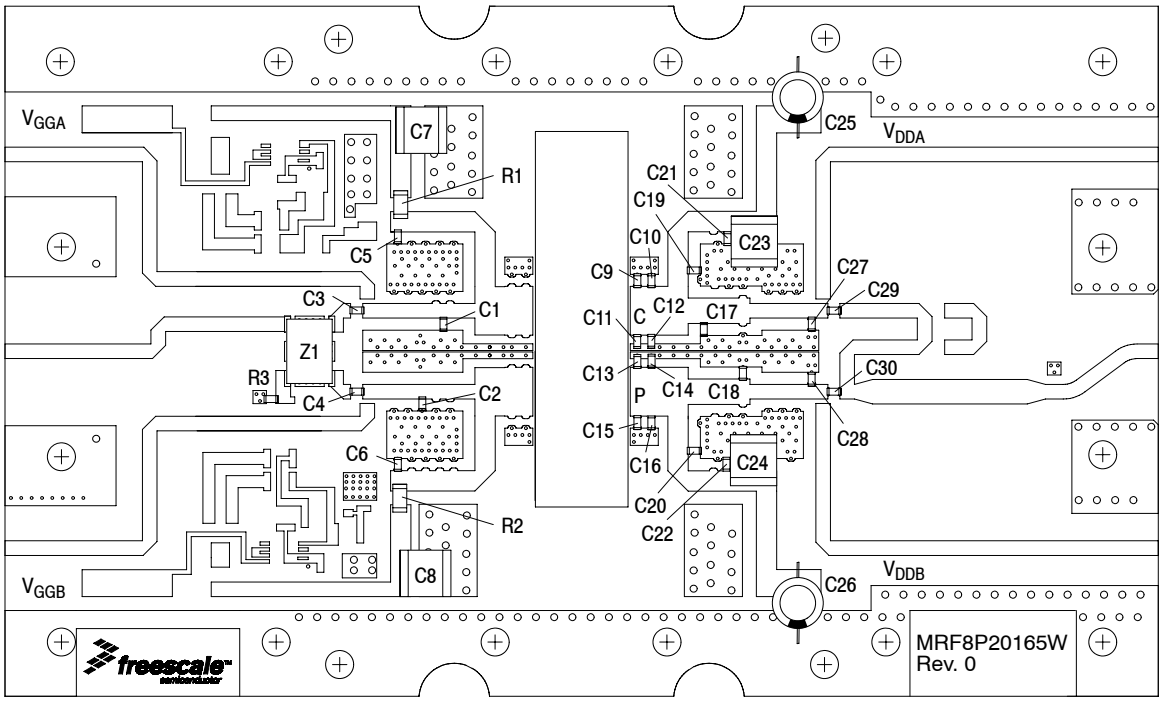


Note 1: Component numbers C5, C17, C20 and C21 are not used.
Note 2: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. MRF8P20165WHR3(WHSR3) Production Test Circuit Component Layout

Table 5. MRF8P20165WHR3(WHSR3) Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C6, C7, C12, C13	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C3, C4	1.8 pF Chip Capacitors	ATC600F1R8BT250XT	ATC
C8, C9, C24, C25	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C10, C11	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C14	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C15, C16	1.0 pF Chip Capacitors	ATC600F1R0BT250XT	ATC
C18, C19	2.0 pF Chip Capacitors	ATC600F2R0BT250XT	ATC
C22, C23	18 pF Chip Capacitors	ATC600F180JT250XT	ATC
C26, C27	0.1 pF Chip Capacitors	ATC600F0R1BT250XT	ATC
C28, C29	220 μF, 50 V Electrolytic Capacitors	227CKS050M	Illinois Capacitor
C30	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
R1	50 Ω, 4 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	2.37 Ω, 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
Z1	1750 MHz Band 90°, 3 dB Hybrid Coupler	GSC351-HYB1900	Soshin
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 3. MRF8P20165WHR3(WHSR3) Characterization Test Circuit Component Layout

Table 6. MRF8P20165WHR3(WHSR3) Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.6 pF Chip Capacitor	ATC600S1R6BT250XT	ATC
C2	1.8 pF Chip Capacitor	ATC600S1R8BT250XT	ATC
C3, C4, C5, C6, C21, C22 C29, C30	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C7, C8, C23, C24	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C9, C11, C13, C15	2.7 pF Chip Capacitors	ATC600S2R7BT250XT	ATC
C10, C12, C14, C16, C17	1 pF Chip Capacitors	ATC600S1R0BT250XT	ATC
C18, C28	0.6 pF Chip Capacitors	ATC600S0R6BT250XT	ATC
C19, C20	1.5 pF Chip Capacitors	ATC600S1R5BT250XT	ATC
C25, C26	330 μF, 35 V Electrolytic Capacitors	MCGPR35V337M10X16-RH	Multicomp
C27	0.5 pF Chip Capacitor	ATC600S0R5BT250XT	ATC
R1, R2	2.37 Ω, 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
R3	51 Ω, 1/4 W Chip Resistor	CRCW120651R0FKEA	Vishay
Z1	1900 MHz Band 90°, 3 dB Hybrid Coupler	GSC351-HYB1900	Soshin
PCB	0.030″, ε_r = 3.48	RO4350	Rogers

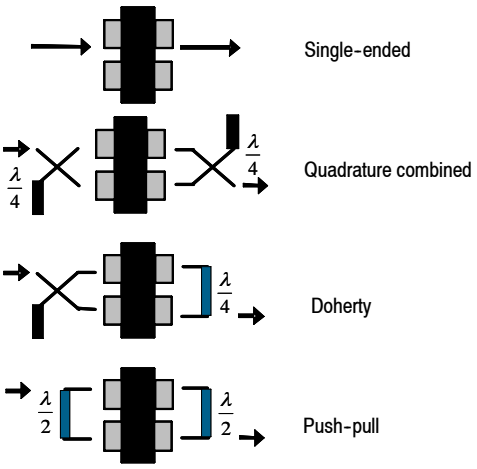


Figure 4. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

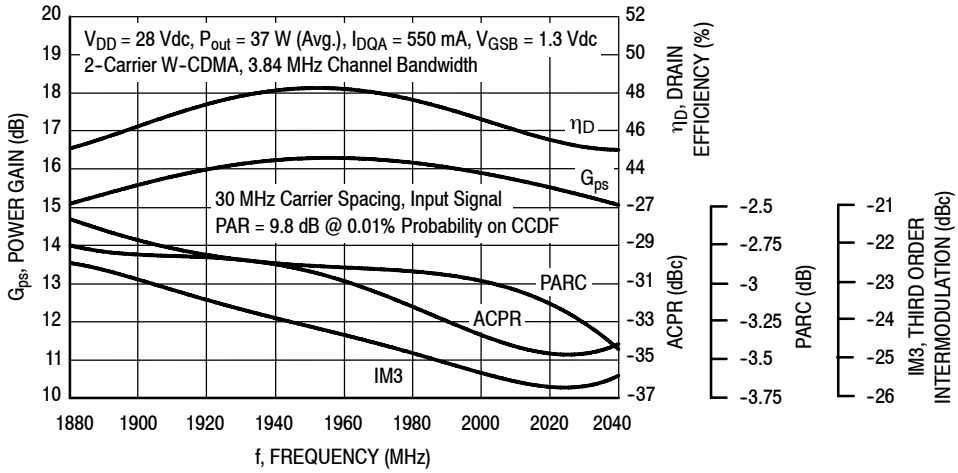


Figure 5. 2-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 37 Watts Avg.

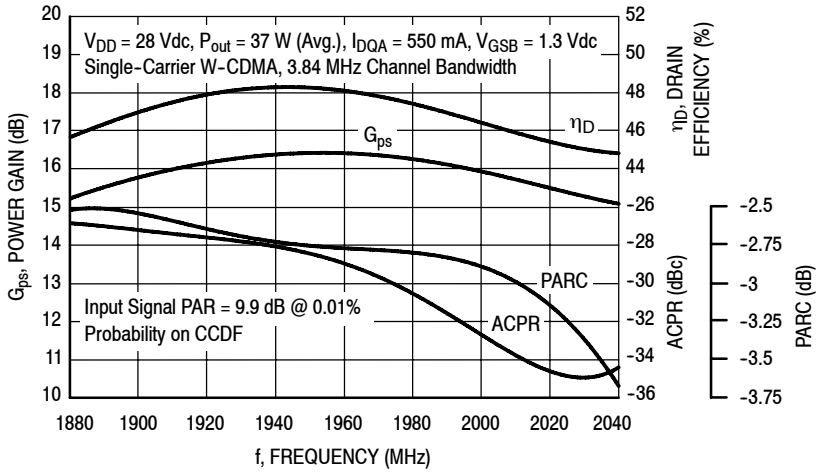


Figure 6. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 37 Watts Avg.

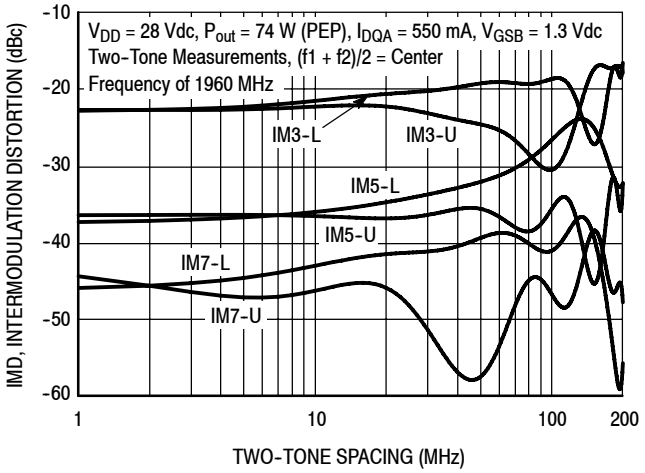


Figure 7. Intermodulation Distortion Products versus Two-Tone Spacing

TYPICAL CHARACTERISTICS

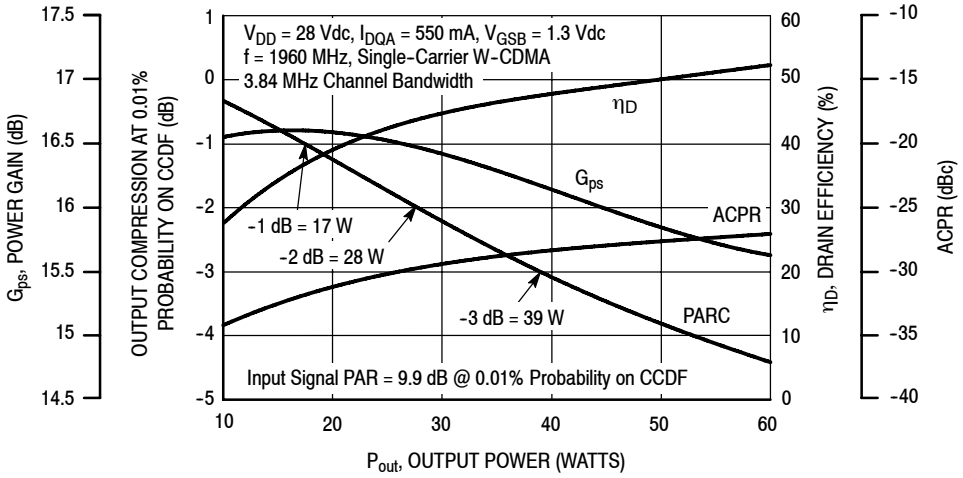


Figure 8. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

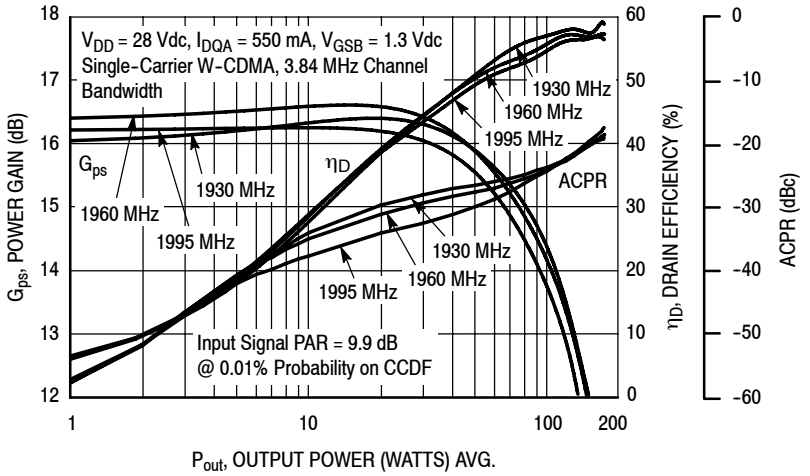


Figure 9. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

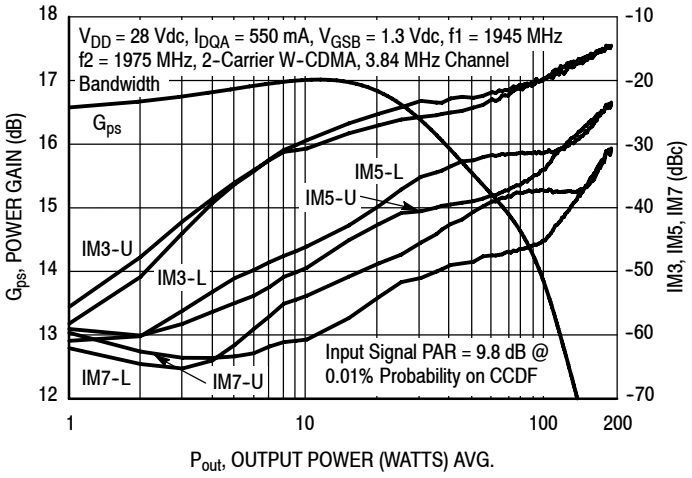


Figure 10. 2-Carrier W-CDMA Power Gain, IM3, IM5, IM7 versus Output Power

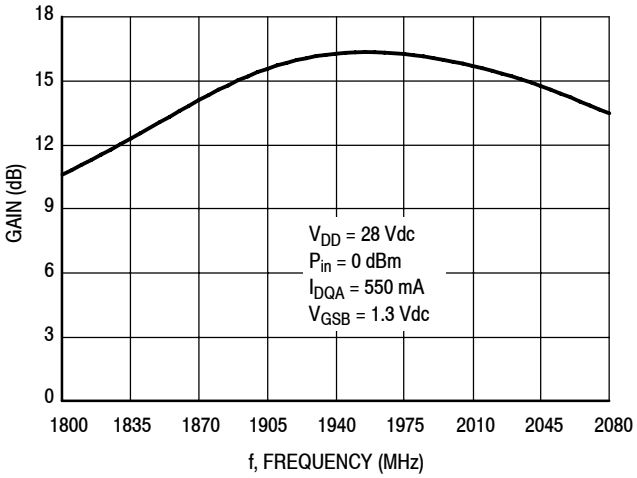


Figure 11. Broadband Frequency Response

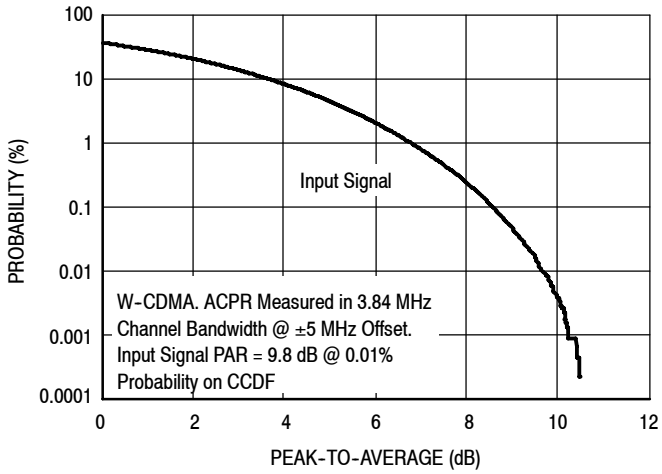


Figure 12. CCDF W-CDMA IQ Magnitude Clipping, 2-Carrier Test Signal

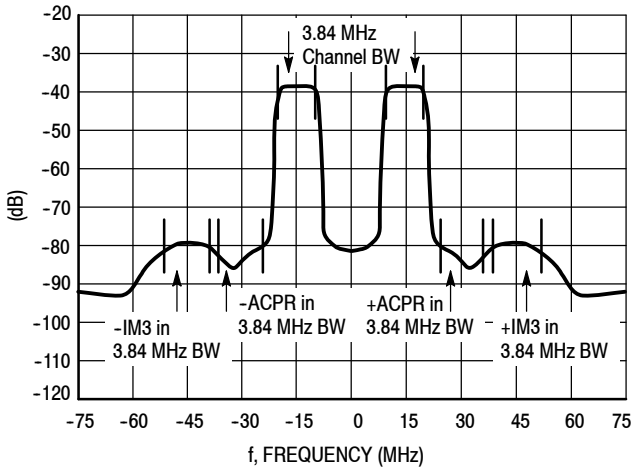


Figure 13. 2-Carrier W-CDMA Spectrum

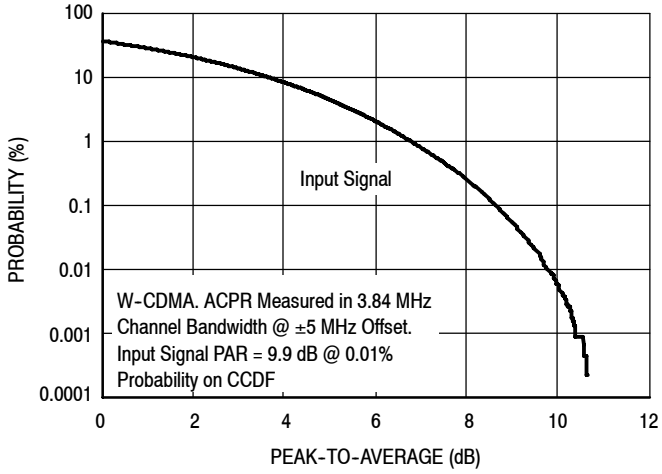


Figure 14. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

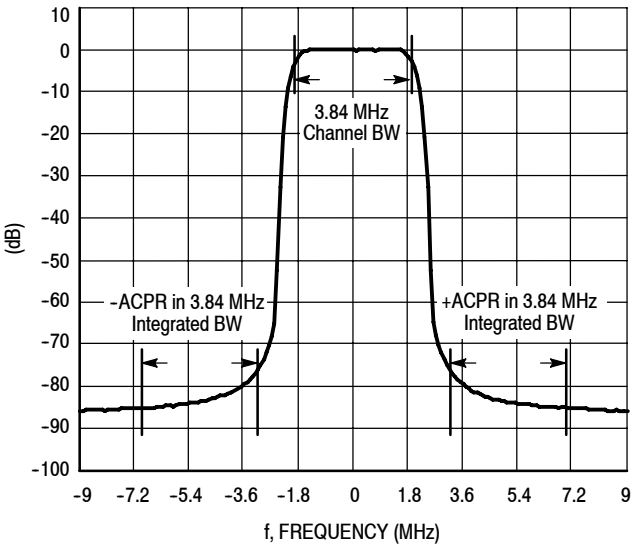


Figure 15. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQA} = 550 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{load} (1) (Ω)	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
1930	16.0 – j8.99	1.58 – j5.68	50.4	110	55.3	51.2	132	55.8
1960	17.2 – j2.43	1.55 – j6.08	50.4	110	54.4	51.3	135	53.5
1990	18.6 + j3.55	1.93 – j5.82	50.4	110	54.4	51.2	132	55.4

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.
Z_{load} = Impedance as measured from drain contact to ground.

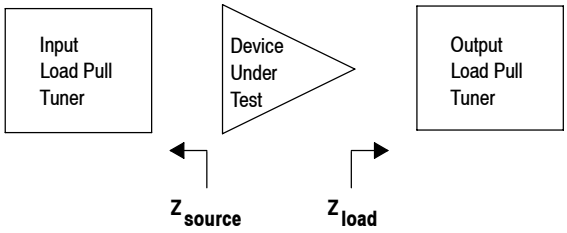


Figure 16. Carrier Side Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQA} = 550 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{load} (1) (Ω)	Max Drain Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
1930	16.0– j8.99	3.45 – j3.43	48.5	71	65.8	49.6	91	66.5
1960	17.2 – j2.43	3.68 – j3.88	48.7	74	65.6	49.6	91	66.1
1990	18.6 + j3.55	2.95– j3.99	48.2	66	65.1	49.6	91	65.3

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.
Z_{load} = Impedance as measured from drain contact to ground.

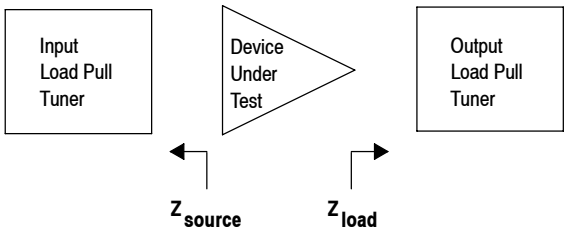
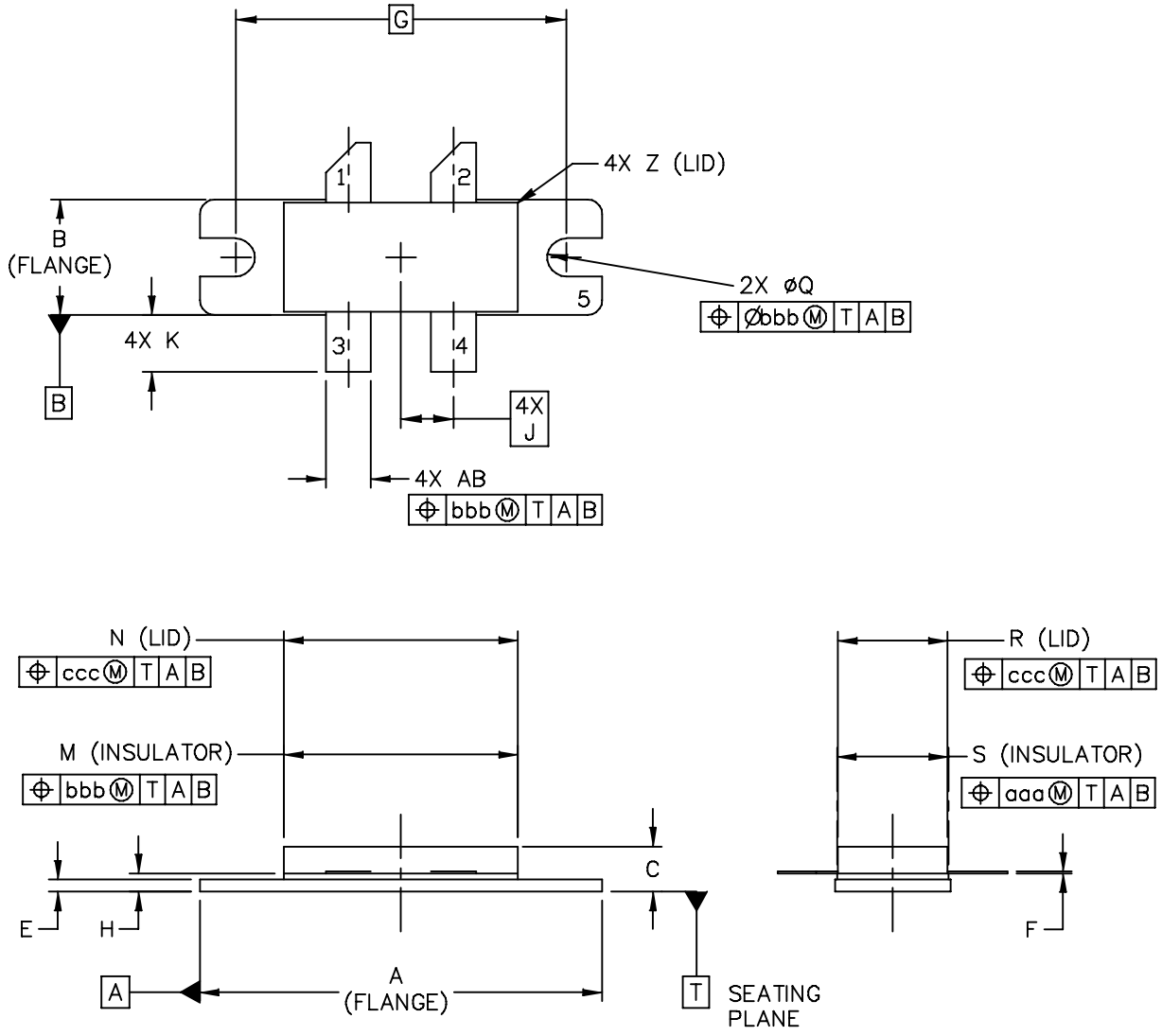


Figure 17. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

PACKAGE DIMENSIONS



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TITLE: NI 780-4	DOCUMENT NO: 98ASA10793D	REV: O
	CASE NUMBER: 465M-01	27 MAR 2007
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa		.005		0.127
J	.175 BSC		4.44 BSC		bbb		.010		0.254
K	.170	.210	4.32	5.33	ccc		.015		0.381
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	ø.118	ø.138	ø3	ø3.51					

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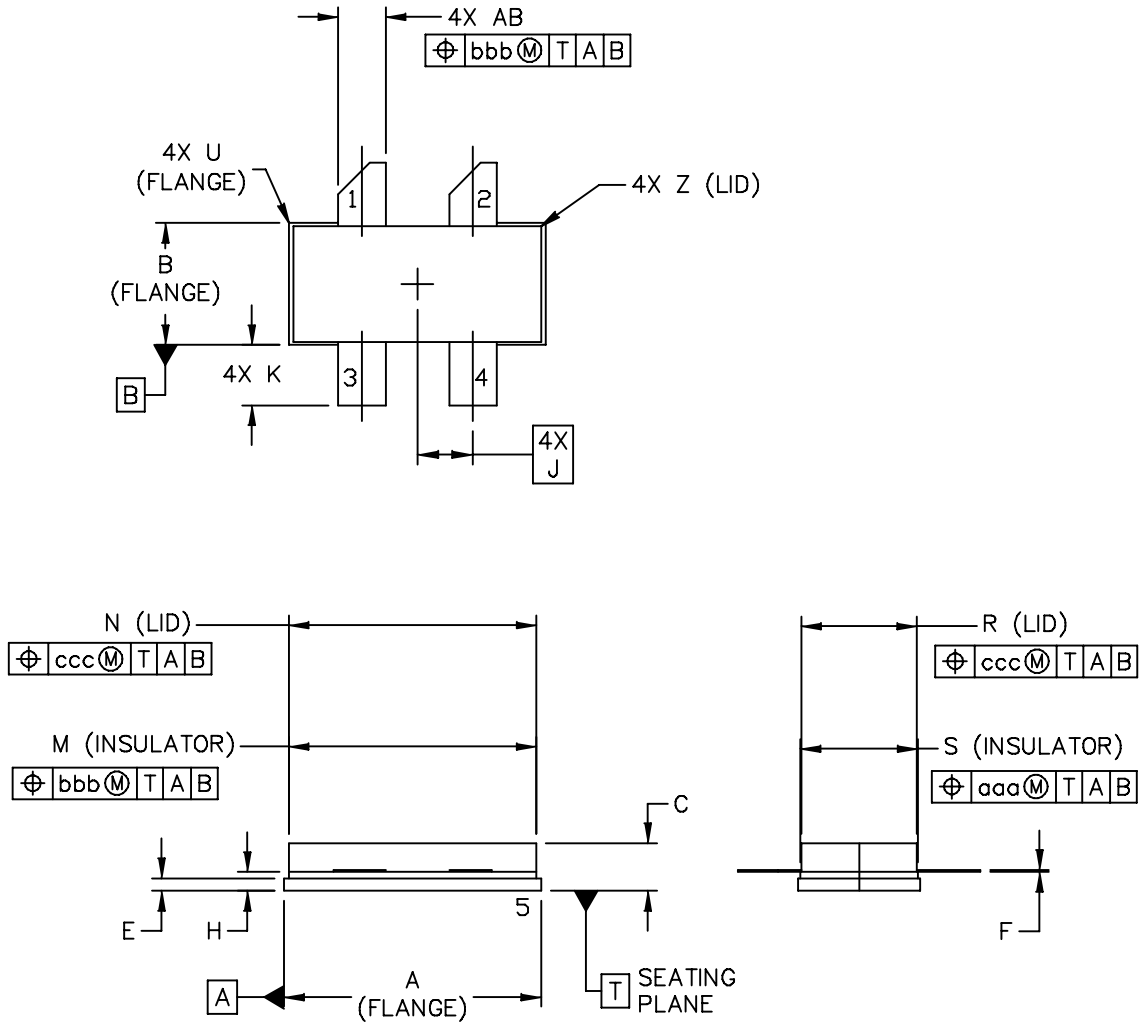

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	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa		.005		0.127
H	.057	.067	1.45	1.7	bbb		.010		0.254
J	.175 BSC		4.44 BSC		ccc		.015		0.381
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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NI 780S–4	CASE NUMBER: 465H–02	27 MAR 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, Software and Tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- .s2p File

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRF8P20165WH and MRF8P20165WHS parts will be available for 2 years after release of MRF8P20165WH and MRF8P20165WHS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRF8P20165WH and MRF8P20165WHS in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2011	• Initial Release of Data Sheet

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